

Engineering INCORPORATING STANDARD CMOS DESIGN PROCESS METHODOLOGIES INTO THE QCA LOGIC DESIGN PROCESS

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As the size and complexity of QCA digital circuits increase, the amount of time needed to create a QCA layout and then perform simulate the quasi-adiabatic switching of that layout significantly increases. To help reduce this development time, the same design process methodology that has been applied in developing CMOS circuits over the past 15 years can be used in the development of QCA circuits. This methodology involves creating and verifying the circuits at higher levels of abstraction before they are implemented and verified at the device level. By following this methodology, QCA circuits can be developed and verified at a behavioral and structural level before they are implemented at a cellular level. Functional errors at these higher levels can quickly be detected and corrected so that when the quasi-adiabatic simulations are performed the circuits will perform properly. By finding these errors early in the process, the overall time to create and verify complex devices should be decreased.

In this paper we will summarize how this methodology was used in the design, layout, and simulation of a medium-sized QCA device that accepts a serial stream of data and monitors the data for a particular serial pattern of bits. VHSIC Hardware Description Language (VHDL) models were developed to represent and verify the QCA circuits before the cellular-level simulation was done. First, behavioral VHDL models were used to verify the input/output operation of the different blocks in the circuit. Then, a VHDL library was created containing design entities that implement the different QCA interactions. This library was used to develop and verify a structural VHDL model that represented the initial QCA layout. Finally, after all the VHDL models were verified, the QCA circuit was then simulated using a more thorough simulation based on quantum mechanics.

Using this methodology resulted in a more efficient design process, as design errors were detected much earlier in the development cycle. A number of functional errors were found and corrected using the VHDL models. This saved development time because those same errors did not propagate through to the more time-intensive cellular level simulations.